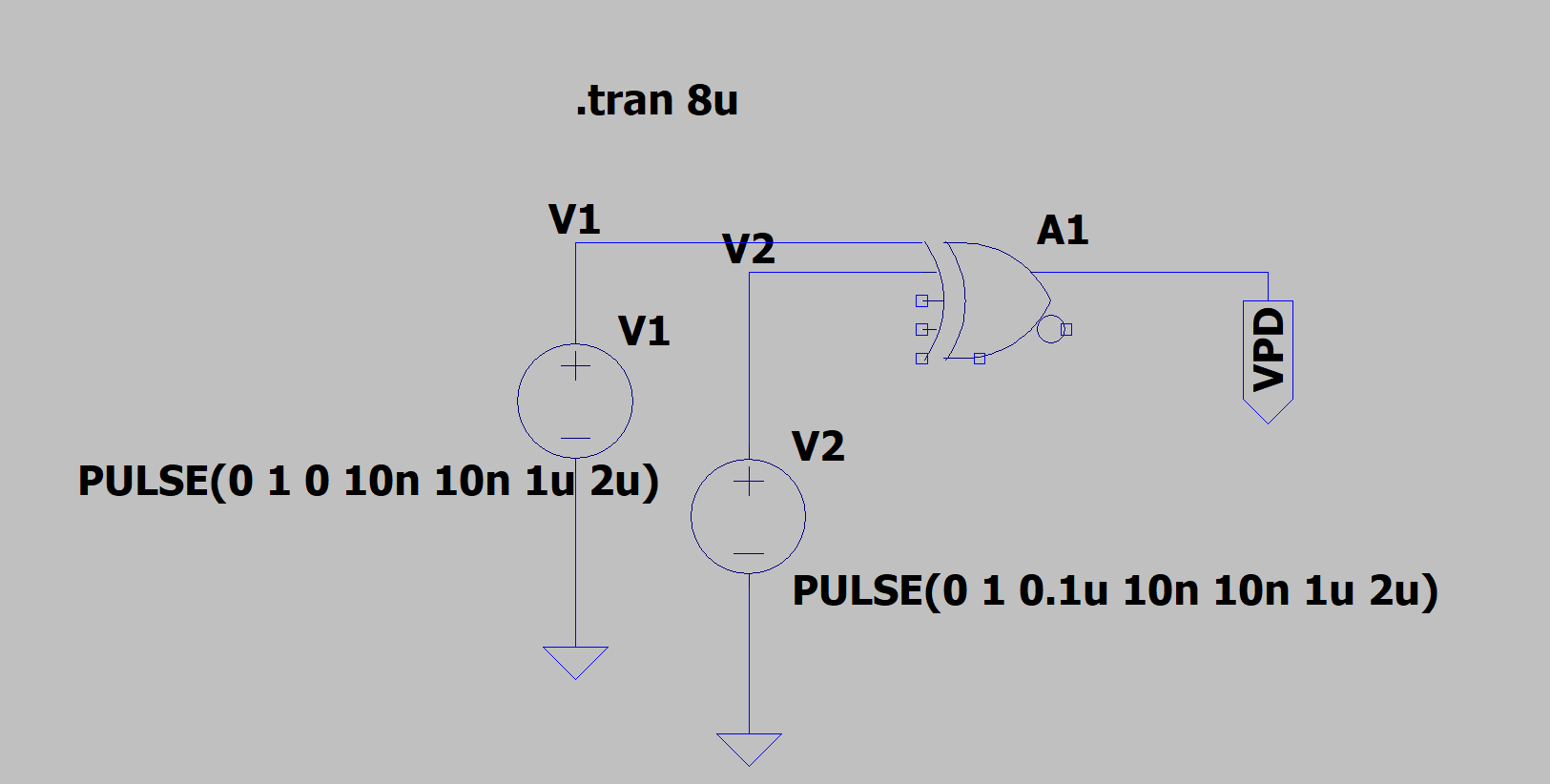
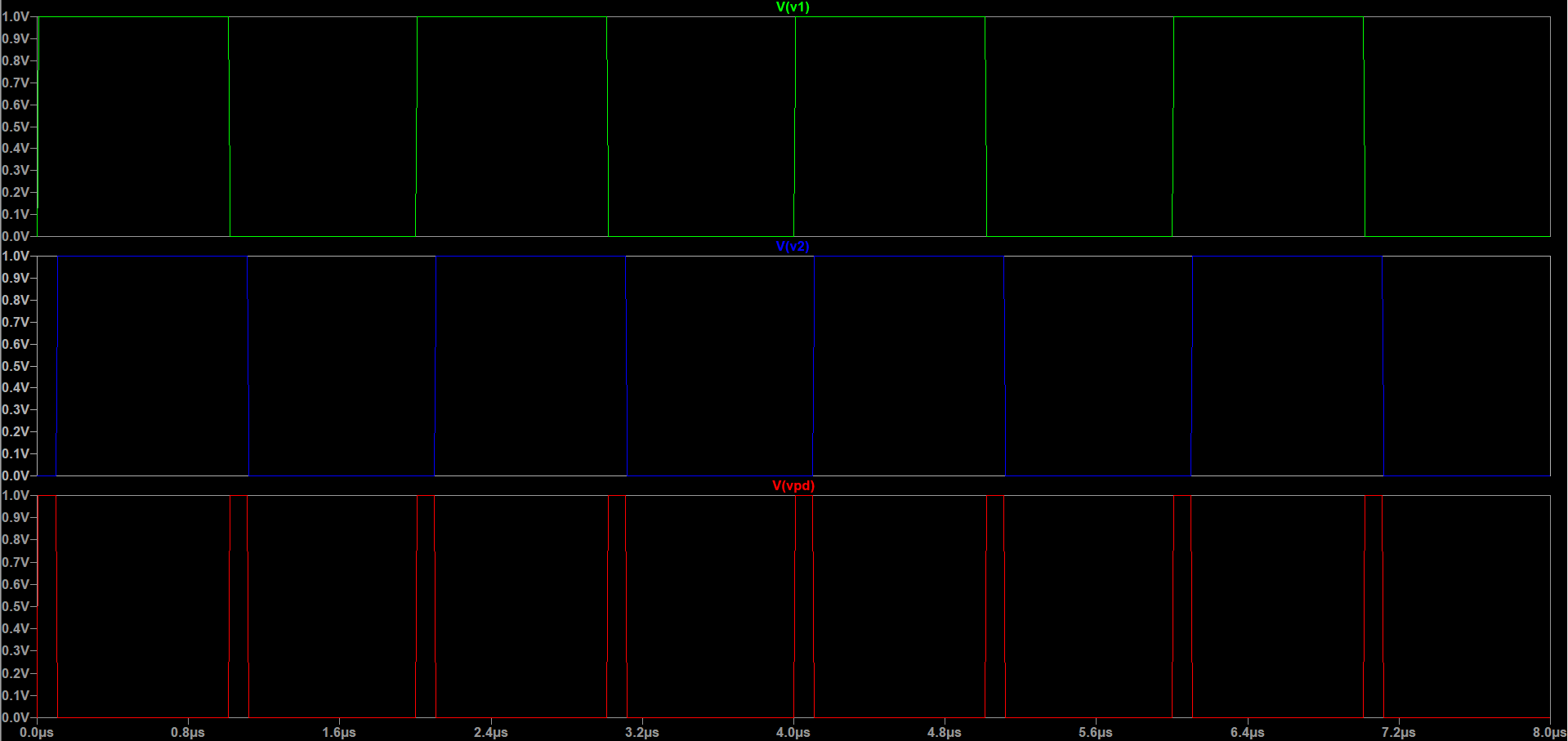
**SIMULATION OF PHASE DETECTOR OF PLL**

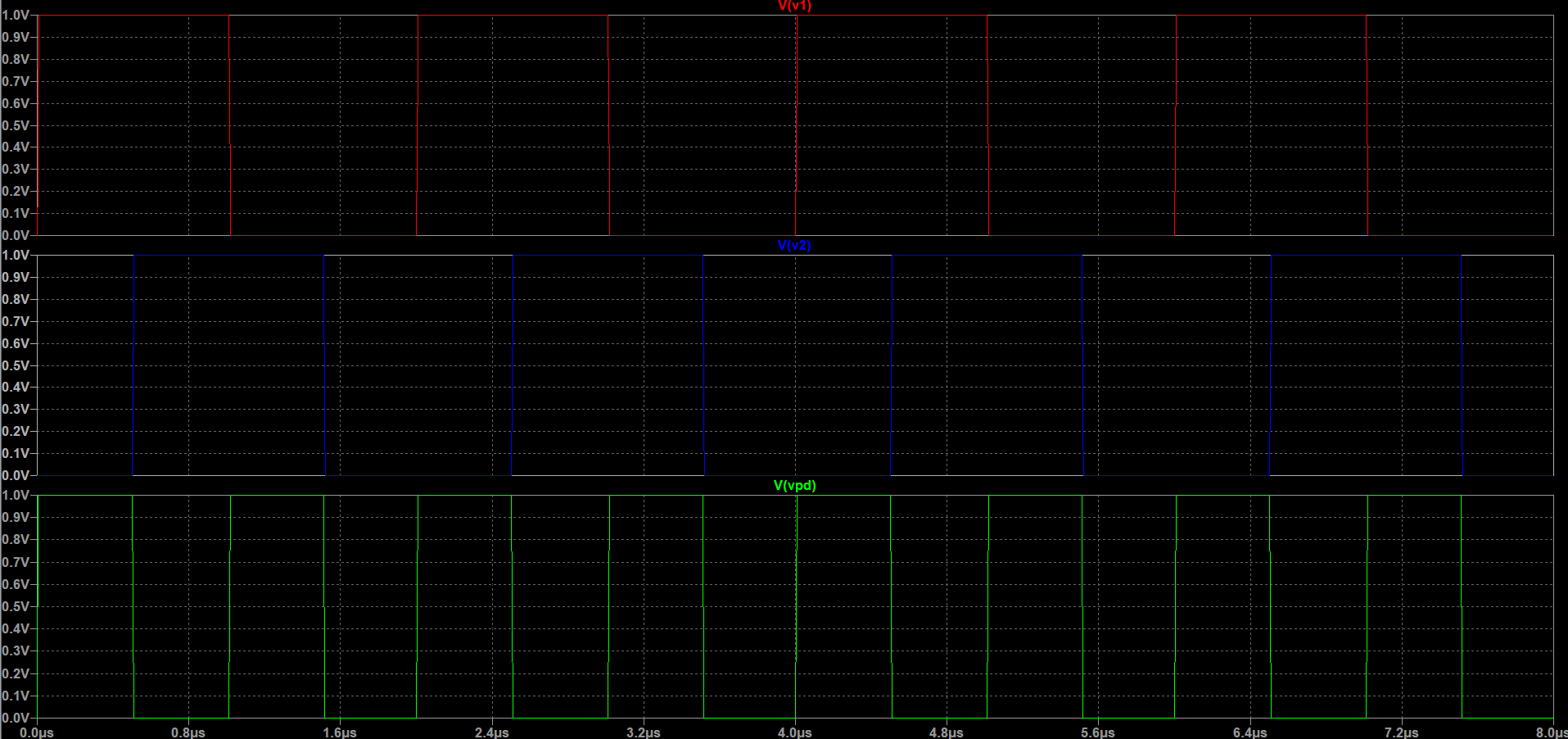
**Circuit Diagram:**

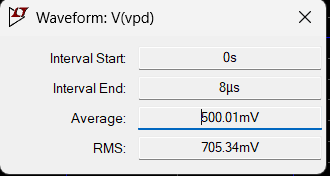


**Output for little delay:**

****

**Output for Delay of Π/2:**

****

****

**Average is 500mv  
phase difference Π/2  
  
So, KPD = 1000\***